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Date of Performance: 28.8.2020
Branch: CSE
Subject Name: Digital Electronics

Aim

Validate truth table for:

- NAND gates HD74LS00
- NOR gates HD74LS02
- NOT gates HD74LS04
- AND gates HD74LS08
- XOR gates HD74LS86

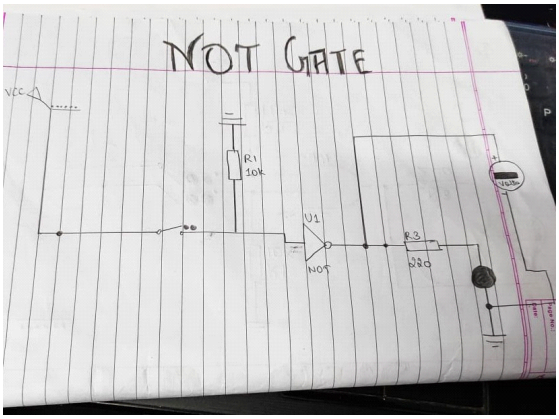
Task to be done

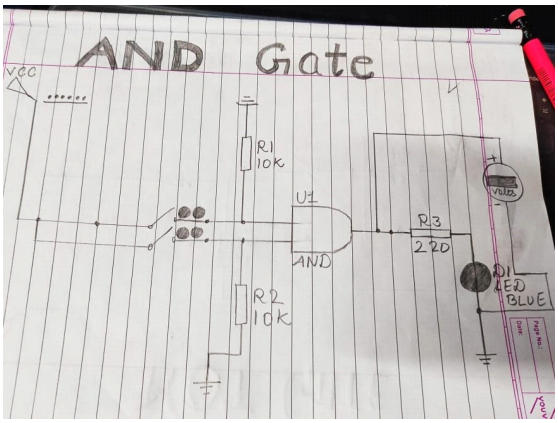
- To verify the truth table of NAND,NOR,NOT,AND,XOR gate*(*HD74LS00,HD74LS02,HD74LS04,HD74LS08,HD74LS86) respectively.

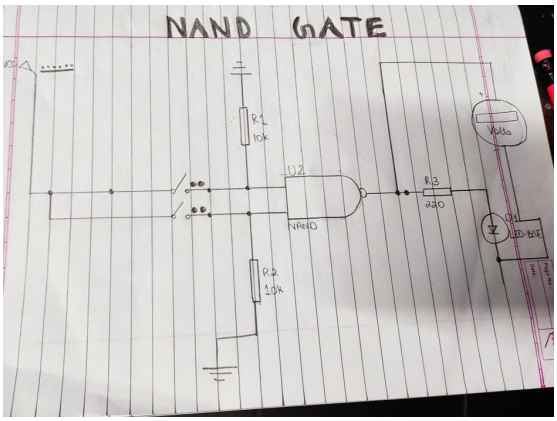
Requirements

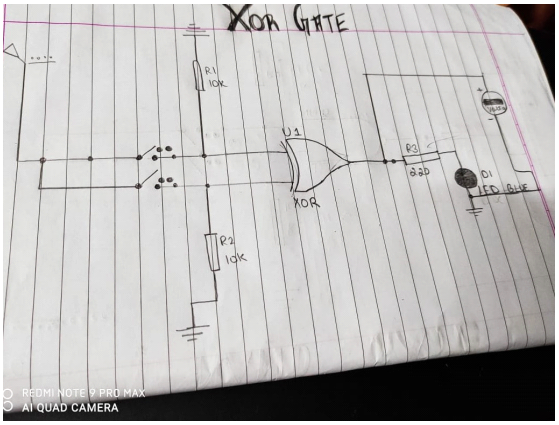
IC for 7400, 7402, 7404, 7408, 7432, 7486, breadboard, connecting wires, 2 momentary switches, two 10 KΩ resistors, 220 Ω resistor, LED.

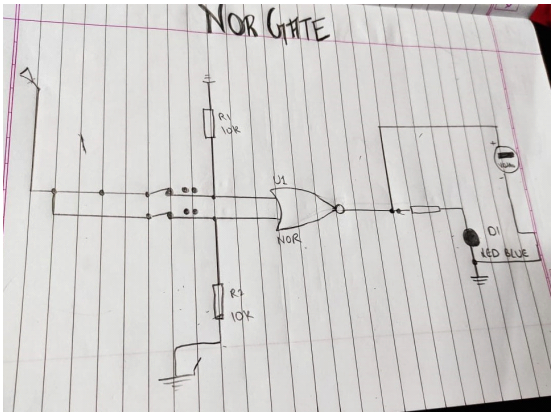
Circuit diagram/ Block diagram





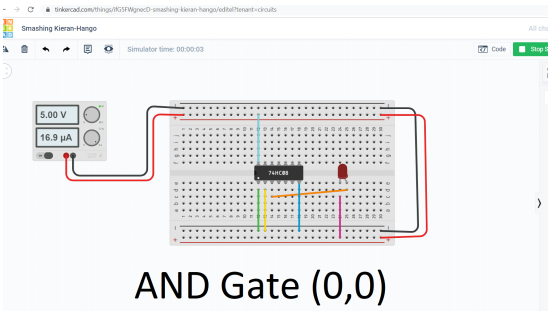




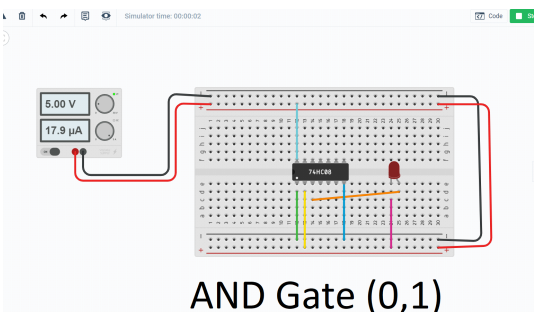


Simulation Results:

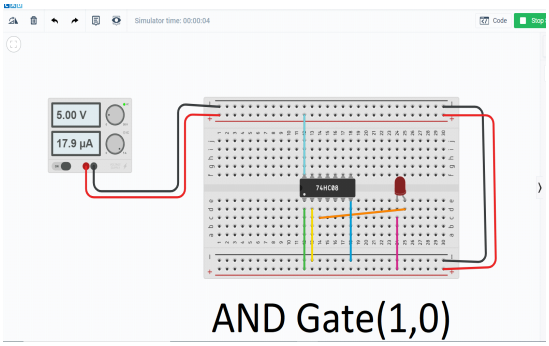
AND GATE-:



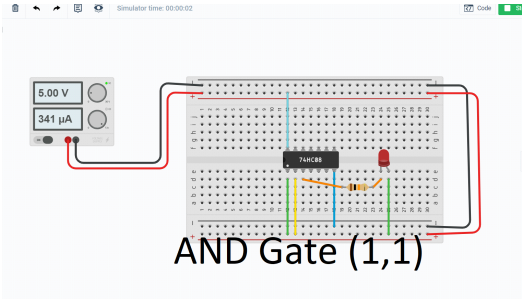
AND Gate (0,0)



AND Gate (0,1)

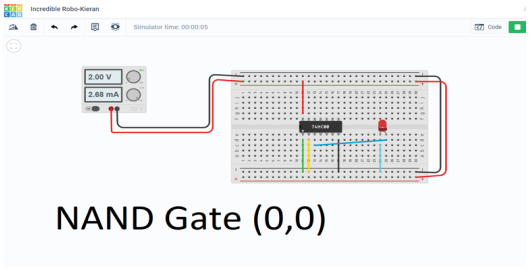


AND Gate(1,0)

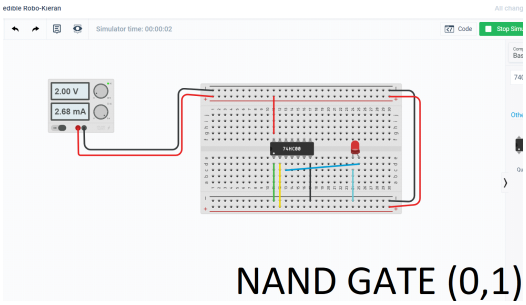


AND Gate (1,1)

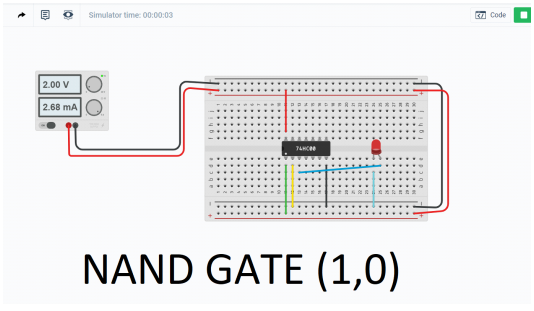
NAND GATE-:



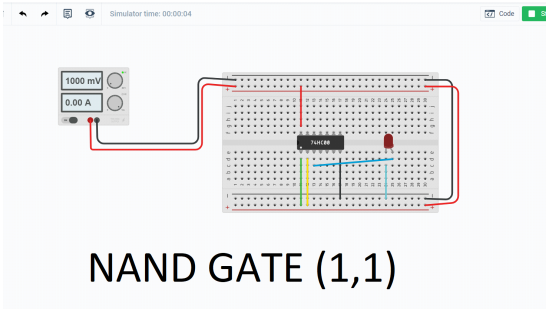
NAND Gate (0,0)



NAND GATE (0,1)

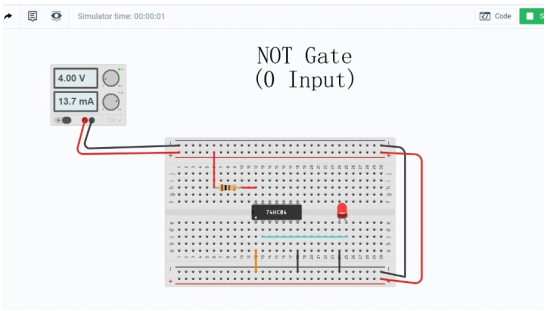


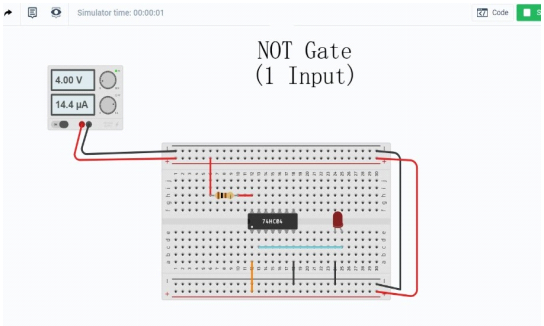
NAND GATE (1,0)



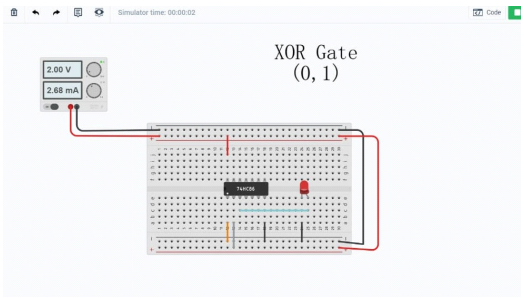
NAND GATE (1,1)

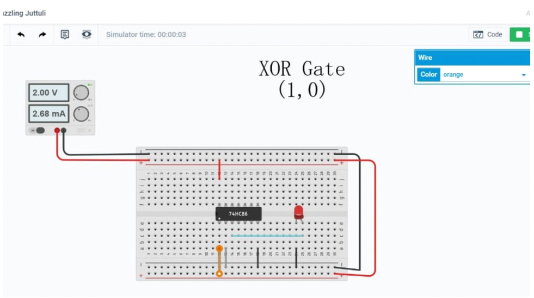
NOT GATE-:

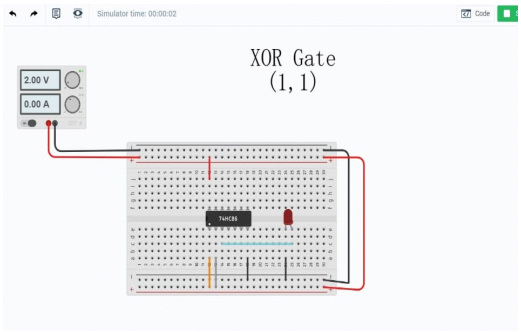


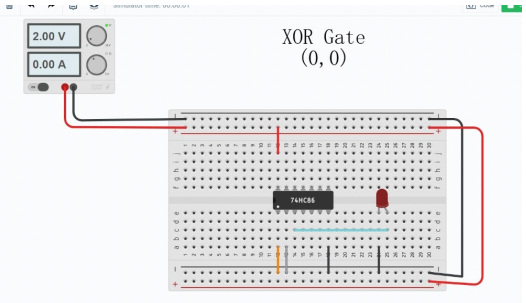


XOR GATE-:









Both inputsHIGH, OUTPUT?

When both inputs are high in case of:-

AND Gate,output is low.

NOR Gate,output is low.

XNOR Gate,output is low.

NAND Gate,output is low.

NOT Gate,output is low.

One inputLOW & other inputHIGH, OUTPUT?

When one input is low and other input is high in case of-:

AND Gate,output is low.

NOR Gate,output is low.

XOR Gate,output is high.

NAND Gate,output is high.

One inputHIGH & other inputLOW, OUTPUT?

When one input is high and other input is low in case of-:

AND Gate,output is low.

NOR Gate,output is low.

XOR Gate,output is high.

NAND Gate,output is high.

Both inputsLOW, OUTPUT?

When both inputs are low in case of-:

AND Gate,output is low.

NOR Gate,output is high.

XOR Gate,output is low.

NAND Gate,output is high.

Concept used

Binary logic deals with binary variables and with operations that assume a logical meaning. It is used to describe in algebraic or tabular form, the manipulation is done by logic circuits called gates. Gates are blocks of hardware that produce graphic symbol and its operation can be described by means of an algebraic expression. The input-output relationship of the binary variables for each gate can be represented in tabular form by a truth-table. Digital logic gates may have more than one input but generally only have one output. Inputs and outputs are in the form of 0(OFF/LOW)and 1(ON/HIGH).

The output state of a digital logic AND gate only returns “LOW” again when ANY of its inputs are at a logic level “0” and LED will not glow. Any LOW input will give a LOW output. The logic or Boolean expression is given for a digital logic AND gate is that for Logical Multiplication which is denoted by a single dot or full stop symbol (.)If both inputs are true, then output is true and LED starts glowing.

The NAND (Not – AND) gate has an output that is normally at logic level “1” and only goes “LOW” to logic level “0” when ALL of its inputs are at logic level “1” . The Logic NAND Gate is the reverse or “Complementary” form of the AND gate. The logic or Boolean expression given for a logic NAND gate is that for Logical Addition, which is the opposite to the AND gate, and which it performs on the complements of the inputs. The Boolean expression for a logic NAND gate is denoted by a single dot or full stop symbol, (.) with a line or Overline, (¯) over the expression to signify the NOT or logical negation of the NAND gate.If either one of the input is NOT true, then output is true and LED starts glowing.

The inclusive NOR (Not-OR) gate has an output that is normally at logic level “1” and only goes “LOW” to a logic level “0” when ANY of its inputs are at logic level “1”. The Logic NOR Gate is the reverse or

“Complementary” form of the inclusive OR gate. The logic or Boolean expression is given for a logic NOR gate is that for Logical Multiplication which it performs on the complements of the inputs. The Boolean expression for a logic NOR gate is denoted by a plus sign, (+) with a line or Overline, (‾‾) over the expression to signify the NOT or logical negation of the NOR gate.If both inputs are NOT true, then output is true and LED starts glowing.

The output of an Exclusive-OR gate ONLY goes “HIGH” when its two input terminals are at “DIFFERENT” logic levels with respect to each other (Fig 6). An odd number of logic “1’s” on its inputs gives a logic “1” at the output and the LED starts glowing.

In case of NOT gate the output is just complement of the input like if input is low or off then ouput is high or on and the LED starts glowing.

Learning/ observation

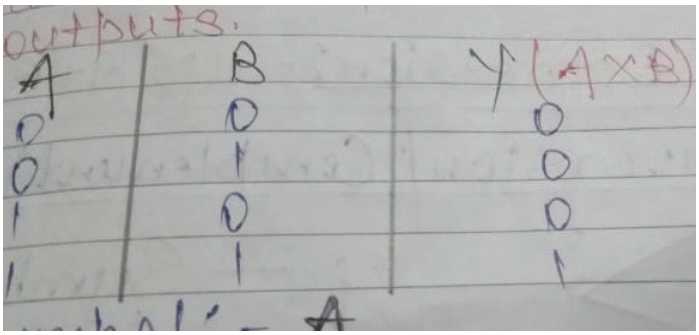
1.AND GATE-:In case of AND GATE:-

(a)When both inputs were low then output was also low and LED did not glow.

(b) When one input was low and other input was high then output was low and LED did not glow.

(c)When one input was high and other input was low then output was low and LED did not glow.

(d)When both the inputs were high then output was also high and LED was glowing.



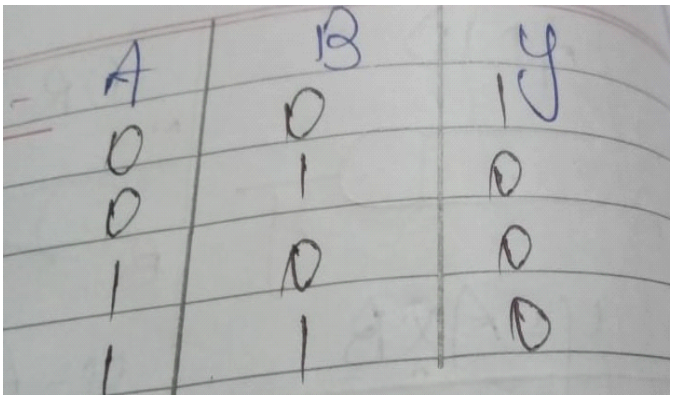
2. **NOR GATE:-In case of NOR GATE-**

(a)When both inputs were low then output was high and LED was glowing.

(b)When one input was low and other input was high then output was low and LED did not glow.

(c)When one input was high and other input was low then output was low and LED did not glow.

(d)When both inputs were high then output was low and LED did not glow.



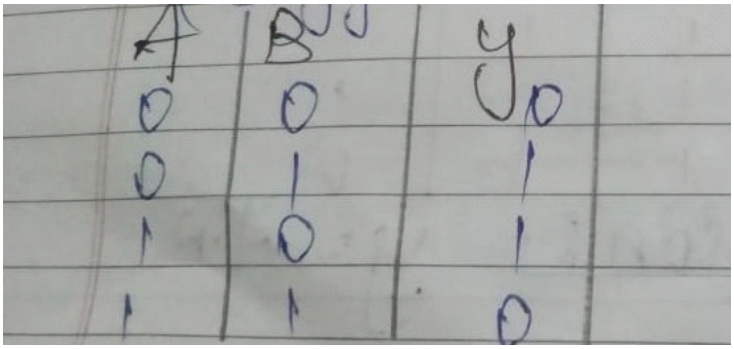
3.XOR GATE:-In case of XOR GATE-

(a)When both inputs were low then output was also low and LED did not glow.

(b)When one input was low and other input was high then output was high and LED was glowing.

(c)When one input was high and other input was low then output was high and LED was glowing .

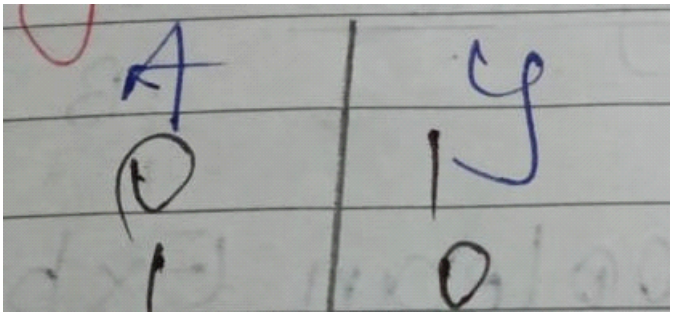
(d)When both inputs were high then output was low and LED did not glow.



4.NOT GATE:-In case of NOT GATE-

(a)When input was low then output was high and LED was glowing .

(b)When input was high then output was low and LED did not glow .



Troubleshooting

Problem occured during the experiment is that on high voltage IC was burstedthen I added resistor in it which prevents IC to get blast.